CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of forming a complementary metal oxide semiconductor structure comprising:

providing a planarized structure comprising a plurality of patterned polysilicon gate regions, each having an exposed upper polysilicon-containing surface, located atop a substrate, said substrate having silicided source/drain contacts formed therein;

forming a first bilayer comprising a first metal-containing layer, said first metal-containing layer is in contact with the exposed upper polysilicon-containing surface of each patterned polysilicon gate region;

patterning said first bilayer to provide a patterned structure in which the first bilayer is removed from preselected patterned polysilicon gate regions;

forming a second bilayer comprising a second metal-containing layer over the patterned structure, said second metal-containing layer is in contact with an exposed upper polysilicon-containing surface of each preselected patterned polysilicon gate regions; and

performing a salicide process that converts the first and second-metal containing layers into metal silicides.

2. The method of Claim 1 wherein the providing the planarized structure comprises the steps of: forming patterned polysilicon gate regions atop the substrate, forming the silicided source/drain contacts into the substrate, forming a dielectric stack comprising a first dielectric and a second dielectric atop the substrate and the patterned polysilicon gate regions and planarizing the second dielectric.

3. The method of Claim 2 further comprising forming at least one spacer about each patterned polysilicon gate region.

4. The method of Claim 3 wherein said at least one spacer has a thickness that is sufficient to prevent encroachment of said silicide source/drain contacts underneath said patterned polysilicon gate region.

5. The method of Claim 1 wherein the plurality of patterned polysilicon gate regions comprises a polysilicon gate conductor that is doped.

6. The method of Claim 5 wherein the polysilicon gate conductor is doped with a dopant selected from As, P, B, Sb, Bi, In, Al, Tl, Ga and mixtures thereof.

7. The method of Claim 1 wherein the silicided source/drain regions are formed using a salicide process which comprises depositing a metal atop activated source/drain regions located in the substrate, first annealing to form a metal silicide, selectively etching non-reacted metal, and optionally performing a second anneal.

8. The method of Claim 7 wherein the metal is selected from the group consisting of Ti, Ta, W, Co, Ni, Pt, Pd and alloys thereof.

9. The method of Claim 7 wherein the first annealing is performed at a temperature from about 300°C to about 600°C in He, Ar, N_2 or forming gas.

10. The method of Claim 7 wherein the optional second anneal is performed at a temperature from about 600°C to about 800°C in He, Ar, N_2 or forming gas.

11. The method of Claim 1 wherein the first metal-containing layer comprises a metal selected from the group consisting of Ni, Co, Pt, Ti, W, Mo, Ta, and alloys thereof.

12. The method of Claim 11 wherein the first metal-containing layer comprises Co or Ni.

13. The method of Claim 11 wherein the first metal-containing layer further comprises an alloying additive.

14. The method of Claim 13 wherein the alloying additive is selected from the group consisting of C, Al, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Zr, Nb, Mo, Ru, Rh, Pd, Ag, In, Sn, Hf, Ta, W, Re, Ir, Pt and mixtures thereof.

15. The method of Claim 1 wherein the first metal-containing layer is used in the formation of silicide gate contacts.

16. The method of Claim 1 wherein the first metal-containing layer is used in the formation of metal silicide gates.

17. The method of Claim 1 wherein the patterning comprises lithography and etching.

18. The method of Claim 1 wherein the second metal-containing layer comprises a metal selected from the group consisting of Ni, Co, Pt, Ti, W, Mo, Ta, and alloys thereof.

19. The method of Claim 18 wherein the second metal-containing layer comprises Co or N.

20. The method of Claim 18 wherein the second metal-containing layer further comprises an alloying additive.

21. The method of Claim 20 wherein the alloying additive is selected from the group consisting of C, Al, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Zr, Nb, Mo, Ru, Rh, Pd, Ag, In, Sn, Hf, Ta, W, Re, Ir, Pt and mixtures thereof.

22. The method of Claim 1 wherein the second metal-containing layer is used in the formation of silicide gate contacts.

23. The method of Claim 1 wherein the second metal-containing layer is used in the formation of metal silicide gates.

24. The method of Claim 1 wherein the salicide process comprises first annealing to form a metal silicide, selectively etching non-reacted metal, and optionally performing a second anneal.

25. The method of Claim 24 wherein the first annealing is performed at a temperature from about 300°C to about 600°C in He, Ar, N_2 or forming gas.

26. The method of Claim 24 wherein the optional second anneal is performed at a temperature from about 600°C to about 800°C in He, Ar, N_2 or forming gas.